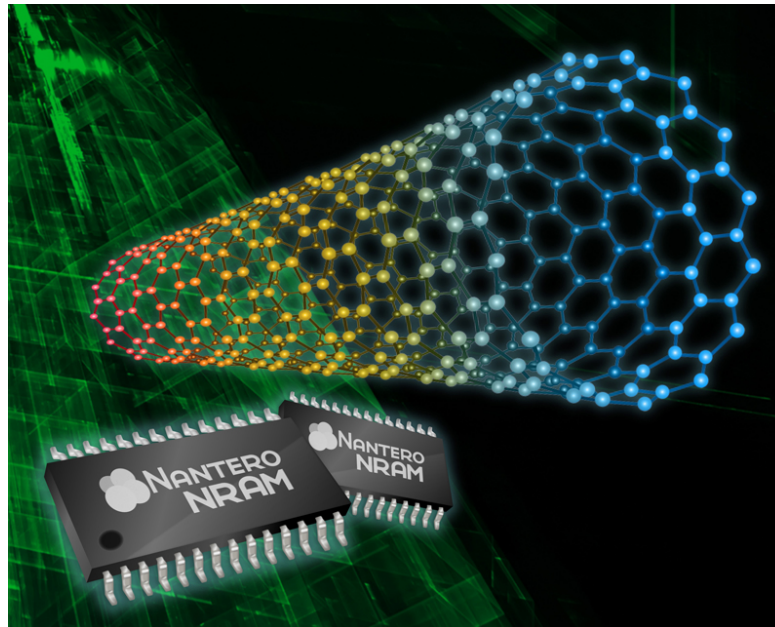


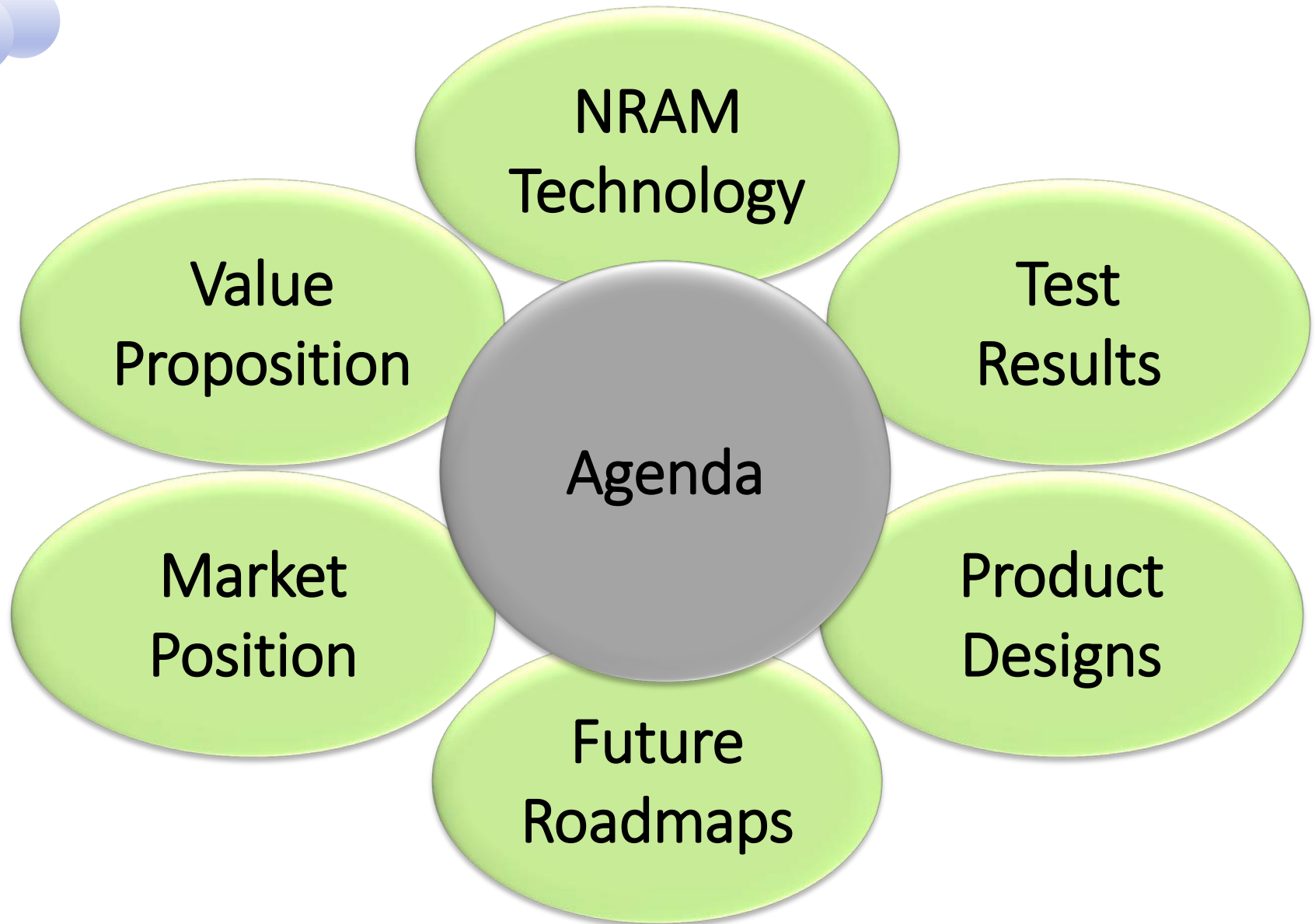


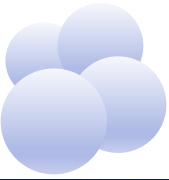
NRAM Defines a New Category of “Memory Class Storage”



Bill Gervasi
Principal Systems Architect

11 April 2019





When was the last time you read about a new volatile memory?

NRAM

MRAM

PCM

3DXP

ReRAM

The non-volatile memory revolution is under way



The Value Proposition for NVRAM is Obvious



Batteries or SuperCaps?
Step on glass or a LEGO?



NVDIMM

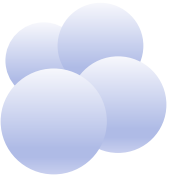
DRAMs used for caches lose data on power fail

An energy store is needed to save data

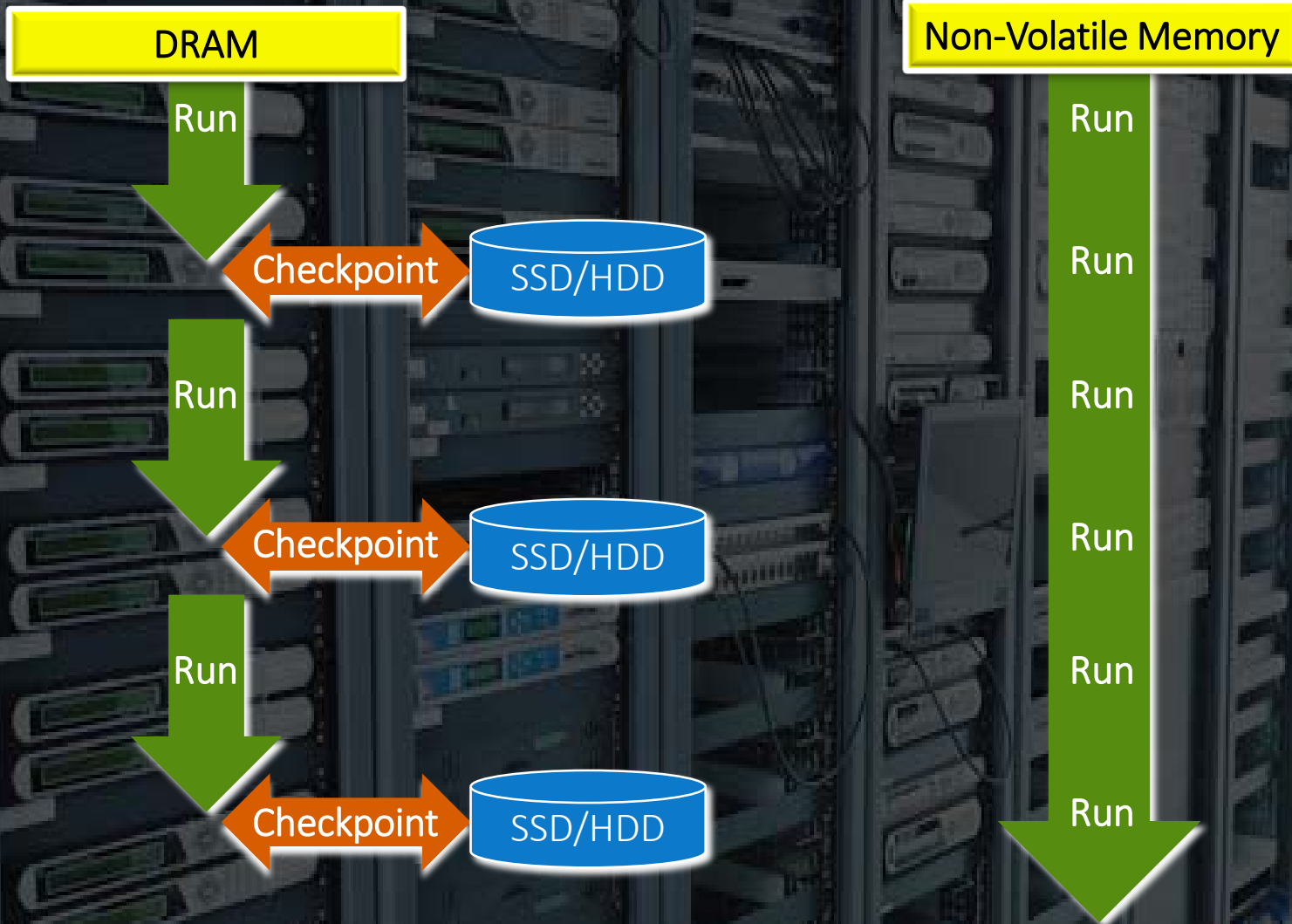
Non-volatile memory eliminates this problem

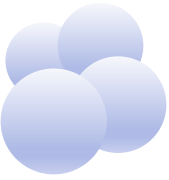


NVMe

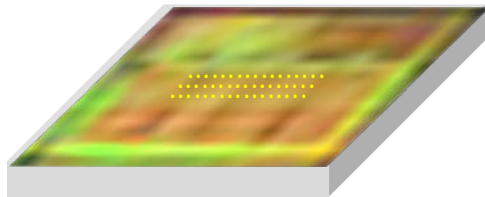


Checkpointing Eats Energy & Performance





Imagine...

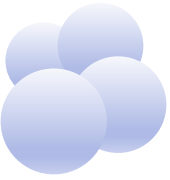


A Non-Volatile

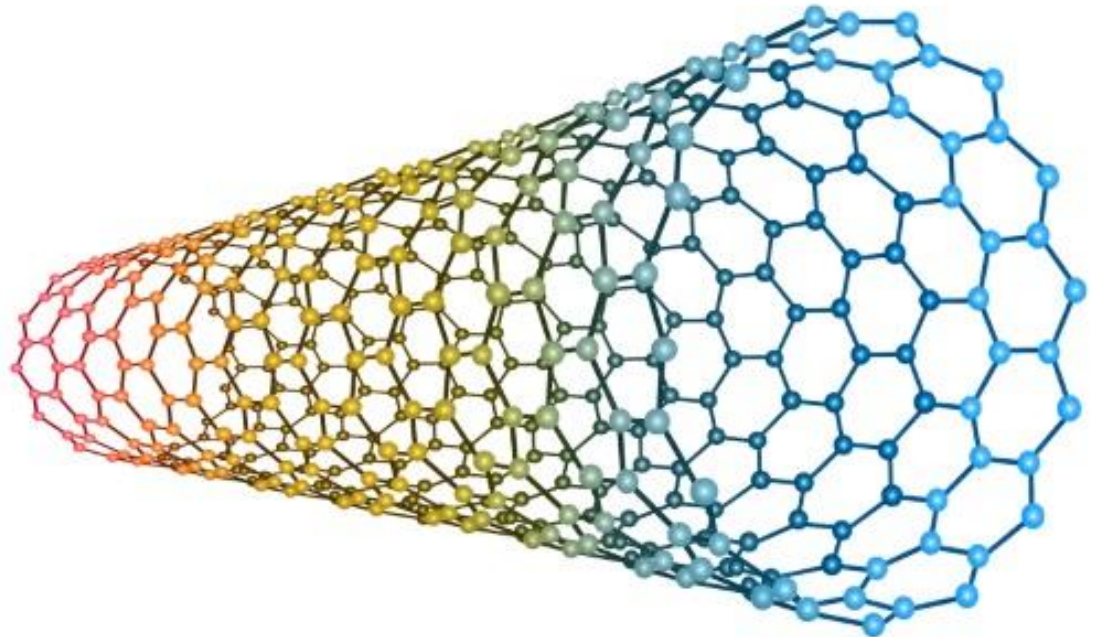
DDR Drop-In

Replacement...





...Using Carbon Nanotubes



With...

High speed

Low volatility

Unlimited write endurance

Wide temperature range

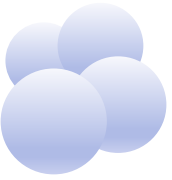
Scalable beyond DRAM

Simple fabric

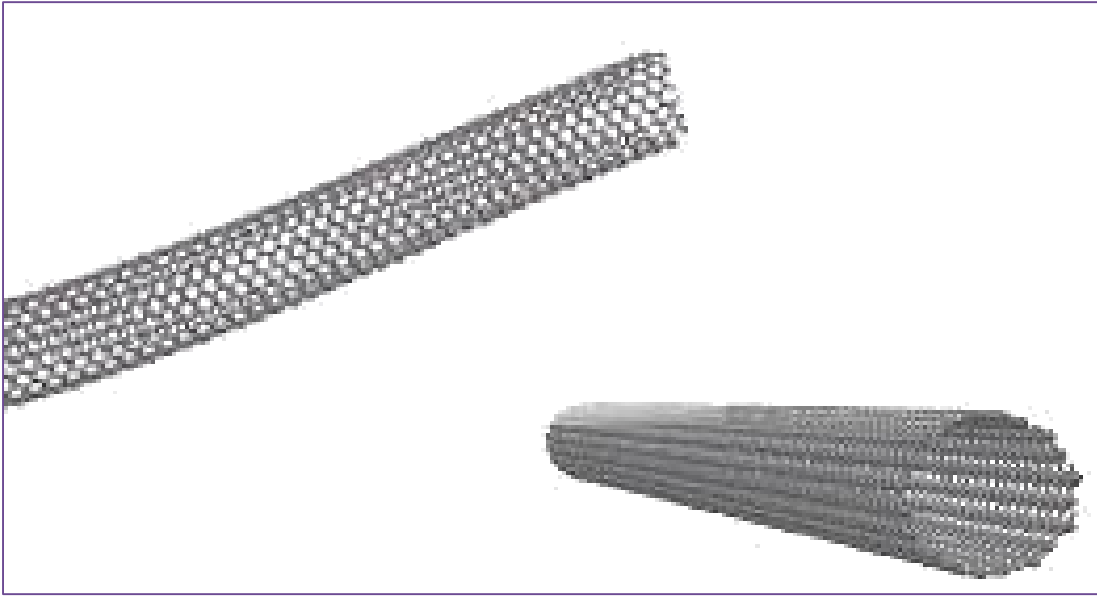
Low power

Low cost





Carbon Nanotubes (CNT)



Nanotubes are in full production today

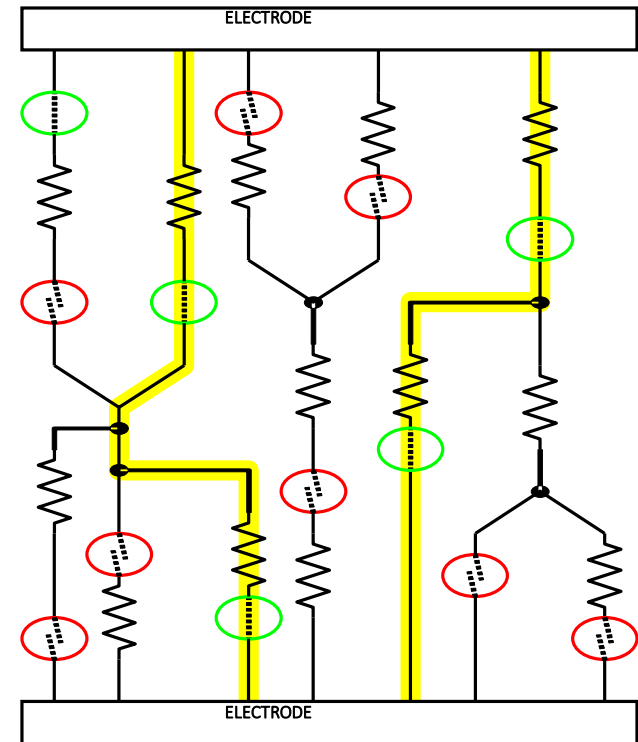
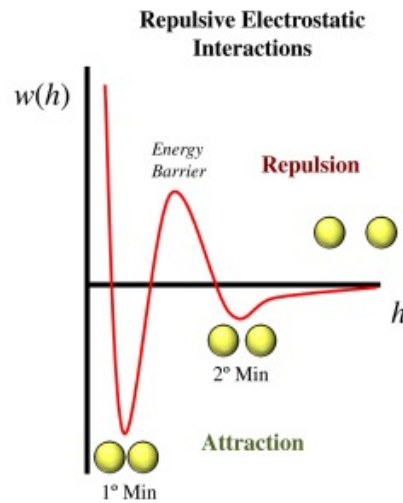
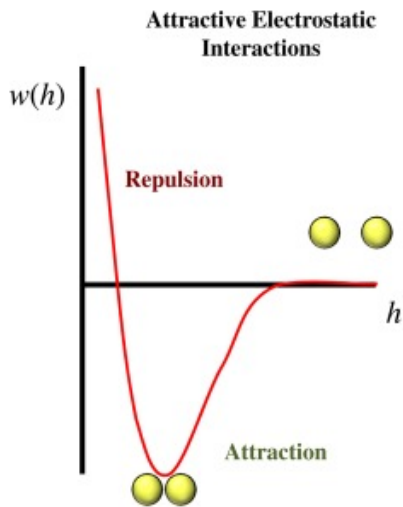
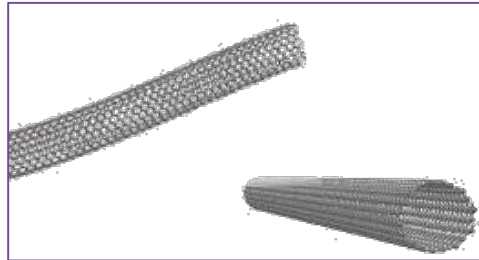
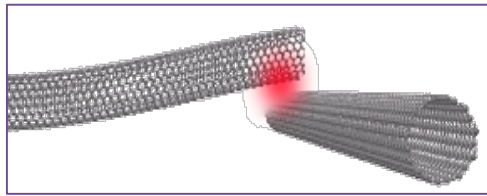
Fundamental resistance is constant

Length and diameter can be selected

Mechanically, thermally, & electrically stable



CNT Nonvolatile Memory Cell

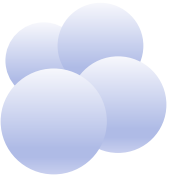


Van der Waals energy barrier keeps CNTs apart or together

Data retention >10 years (more like >1000 years)

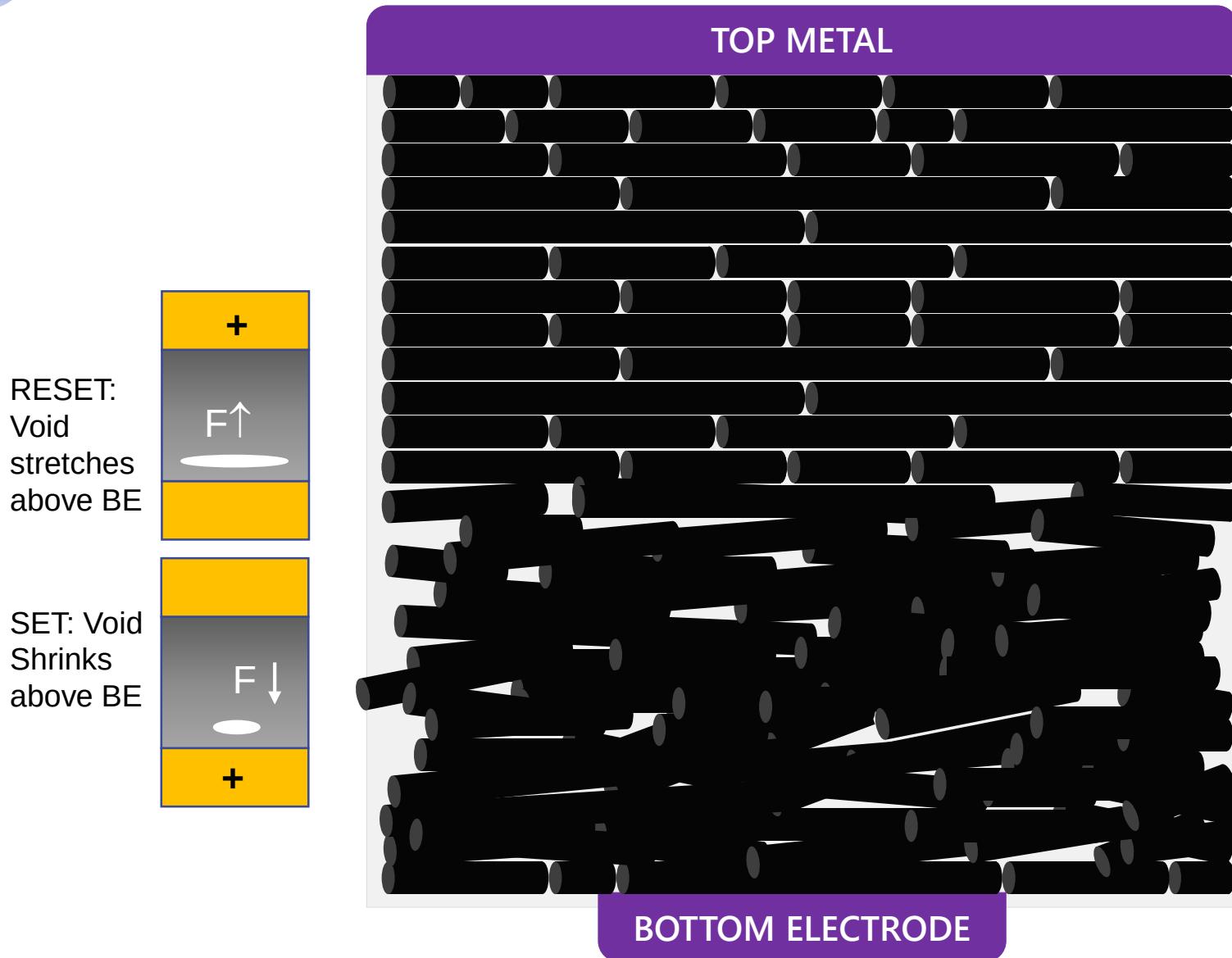
Stochastic array of hundreds nanotubes per each cell



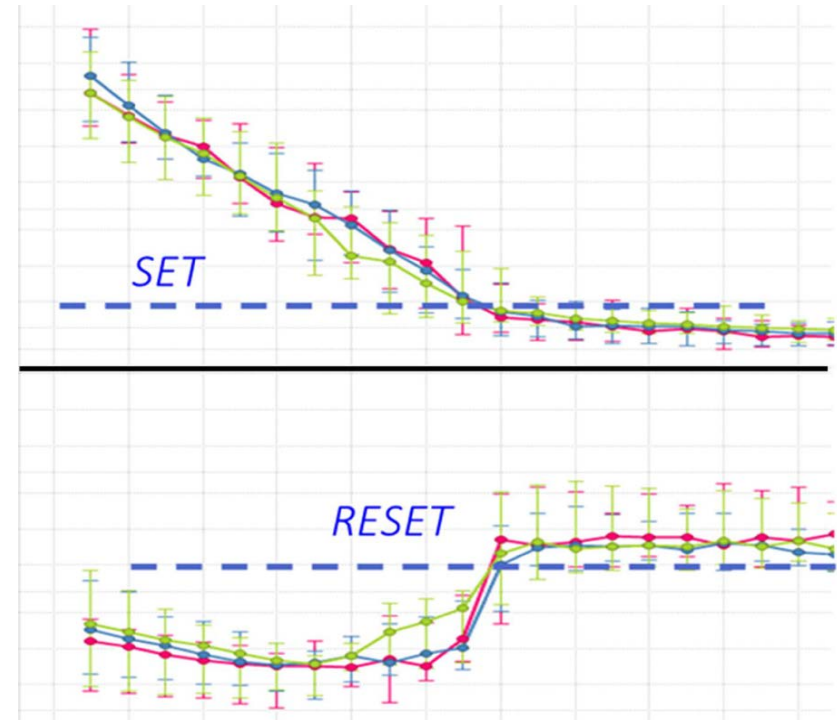
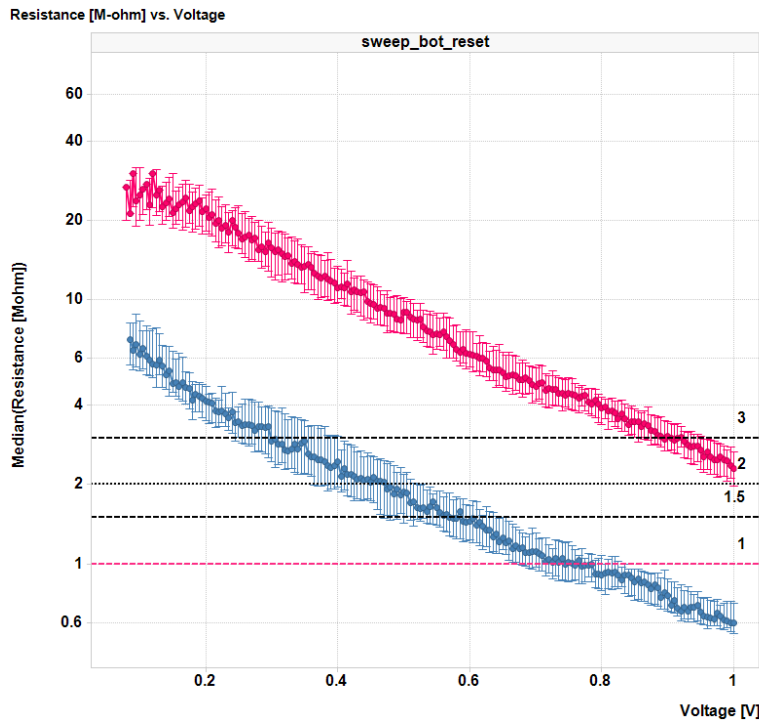


CNT Mechanism Animation

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Resistance Measurements, 0 and 1



No calibration required across the wafer

MLC has been tested as well

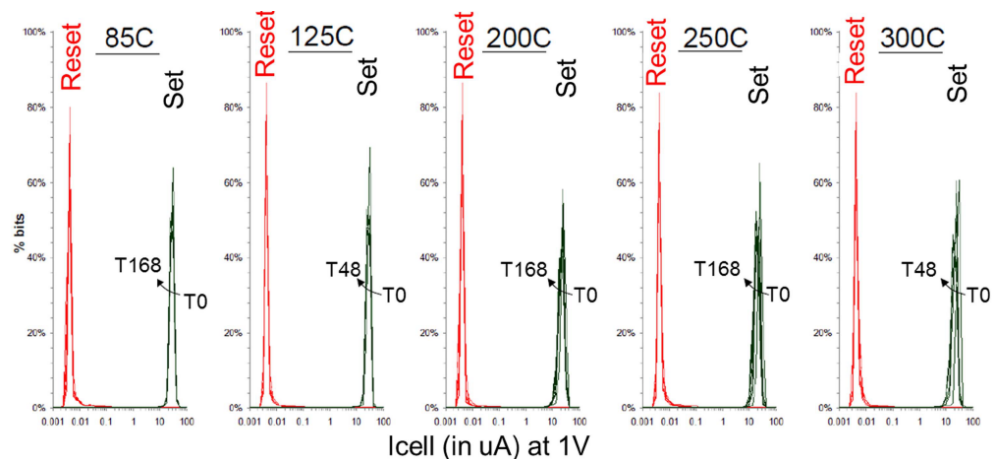


No Temperature Sensitivity in Timing



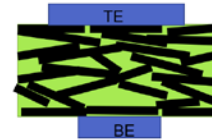
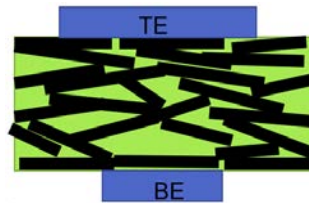
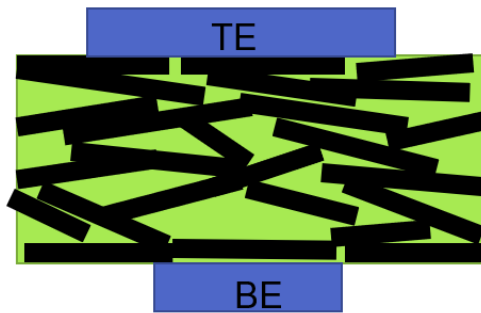
5 ns read/write per cell

No change from -55°C to $+300^{\circ}\text{C}$



No write endurance limits seen in 10^{13} cycles

Scalability

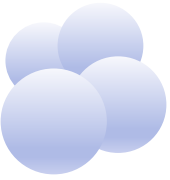


Key factor is the number of CNT junctions per bit (>100 needed)

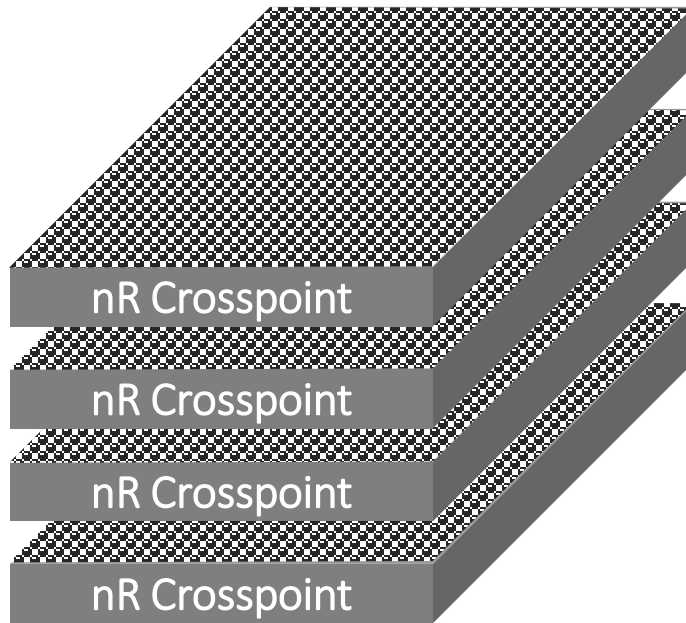
Switching demonstrated from 180nm to 15nm

Modeling shows viability to 1 nm logic process

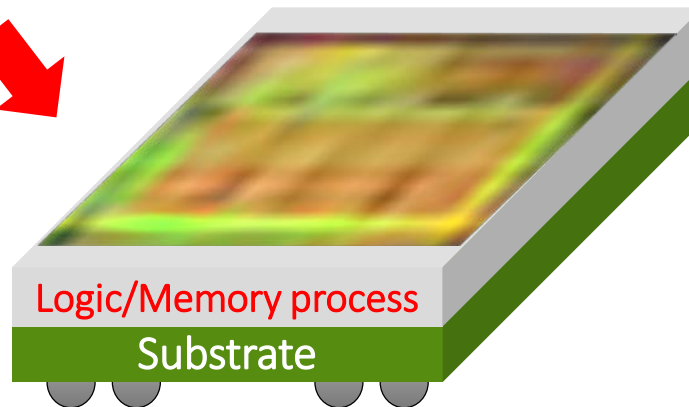
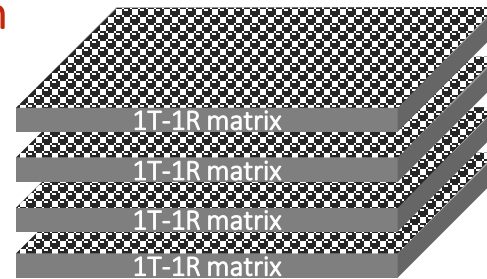




Flexible Fabrication & Application



Either...
Or Both



Function of
Design Efficiency

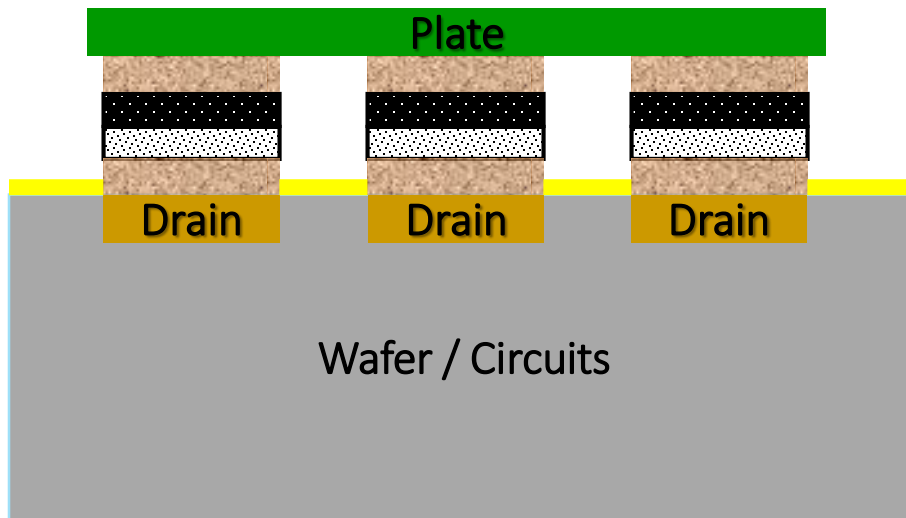
Crossover around
High Mb or low Gb



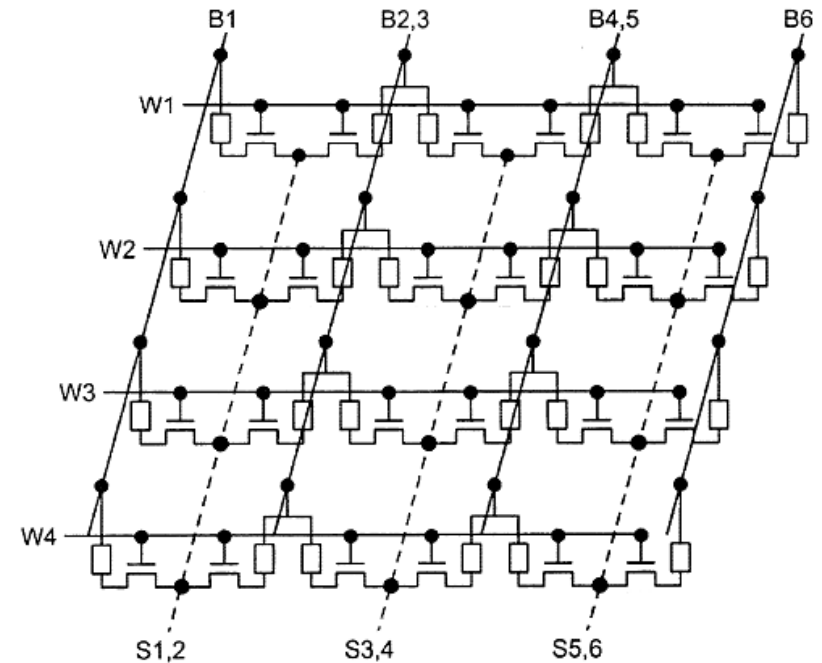


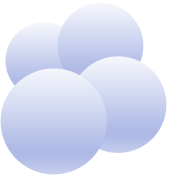
Transistors in the Array

More like traditional DRAM; better for small arrays



1T-1R NRAM in Memory Process

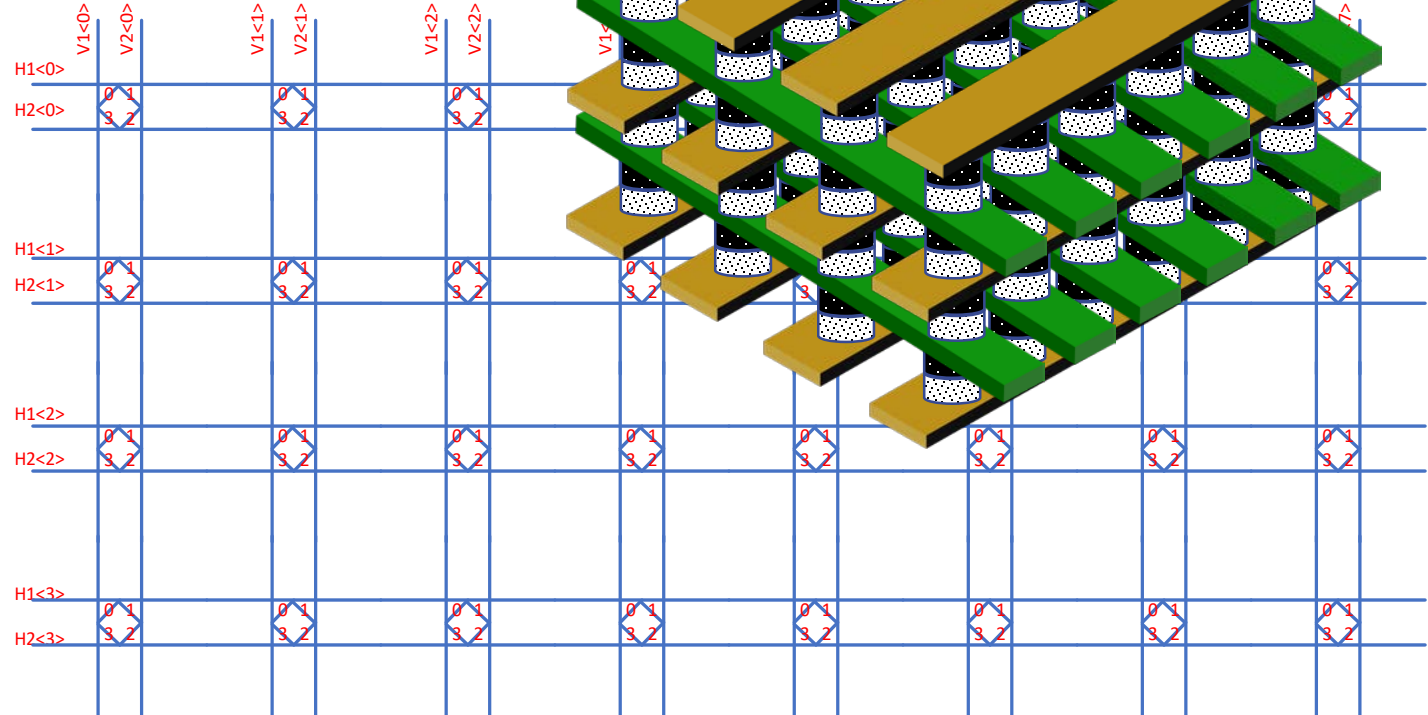
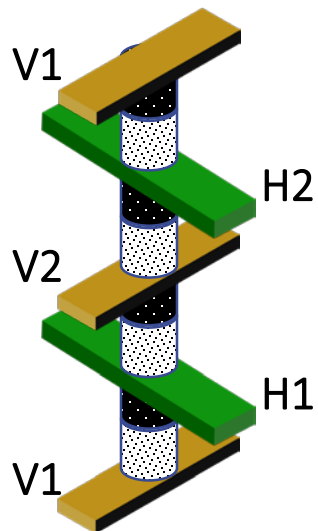




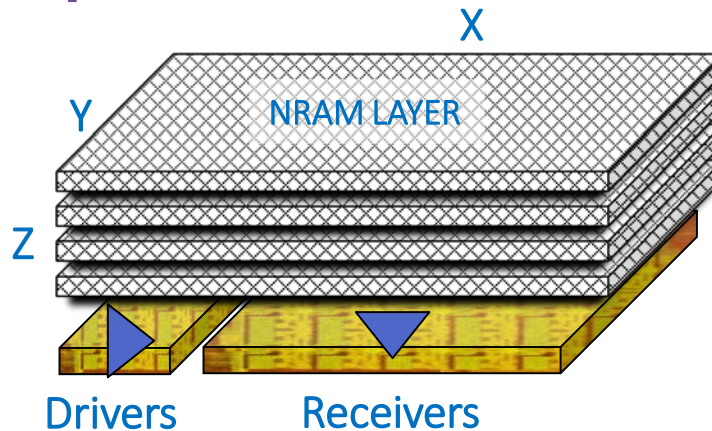
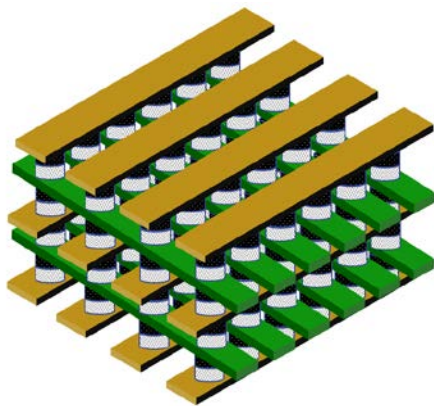
Memory Crosspoint Structure

Cells constructed from resistive elements between lines

Self-selecting due to extremely low leakage

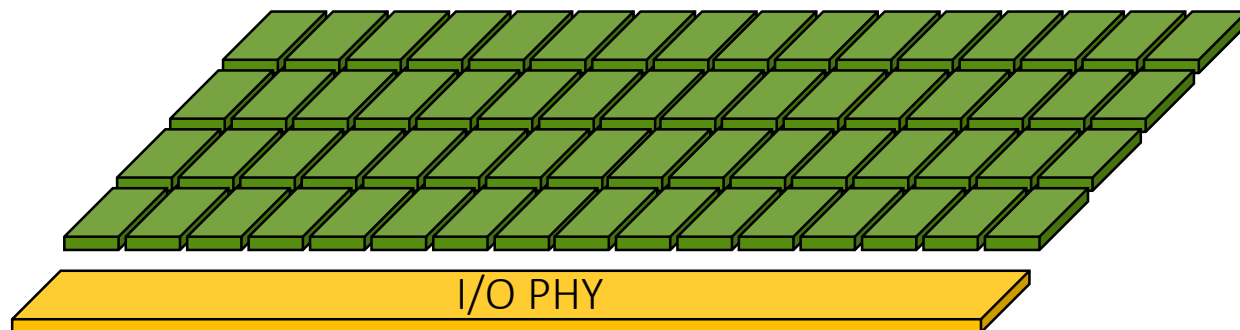


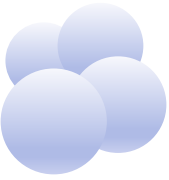
Making a DRAM Replacement With CNT



Tune the array size to the size of drivers & receivers
 Chip-level timing is a function of bit line flight times
 Replicate this “tile” as needed for device capacity
 Add I/O drivers to emulate any PHY needed

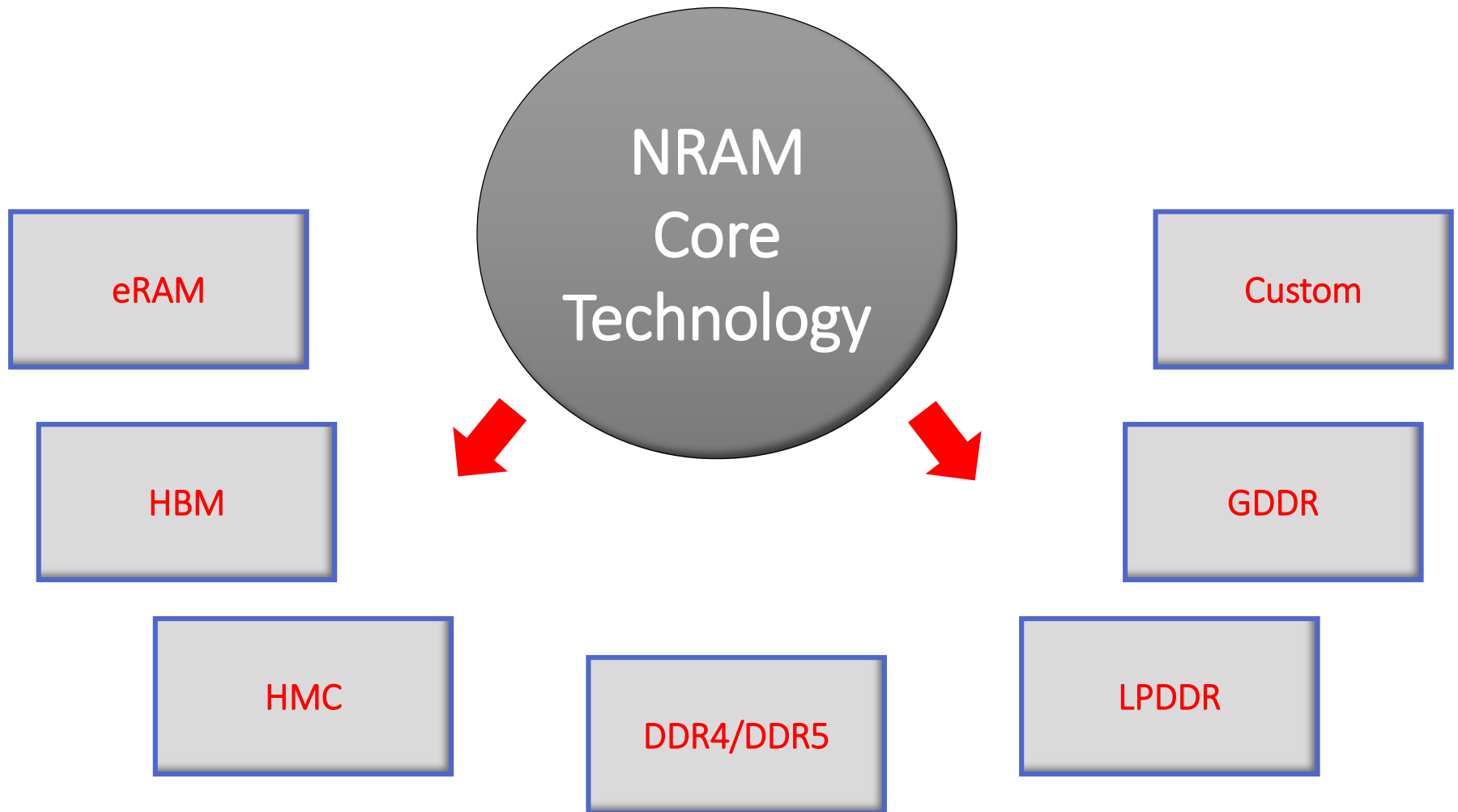
64 Kb tile
 X
 256 K tiles
 =
 16 Gb

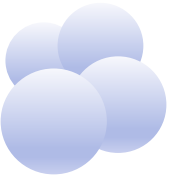




Many I/O Types Possible

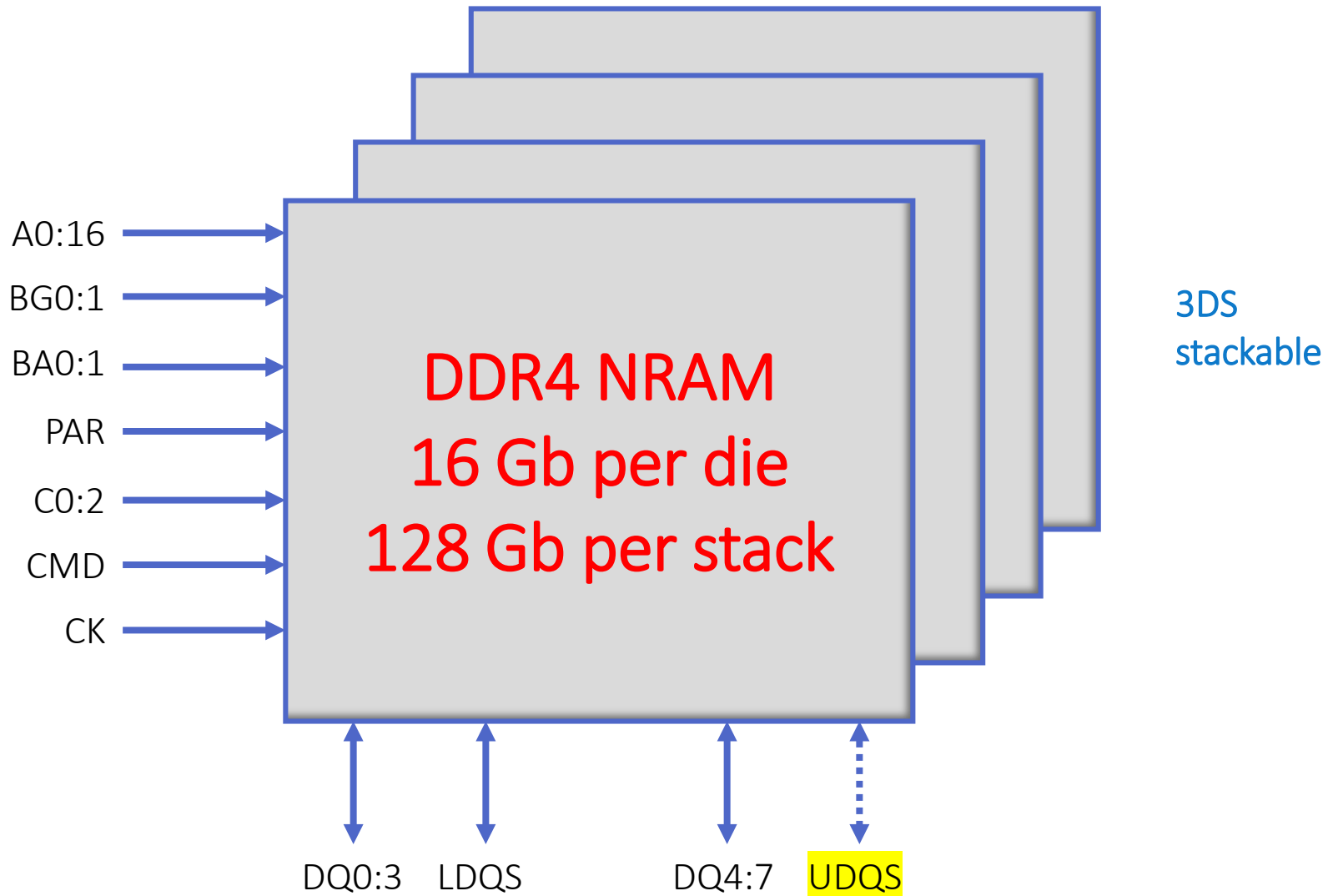
19 |

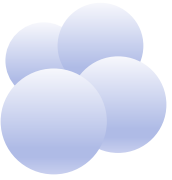




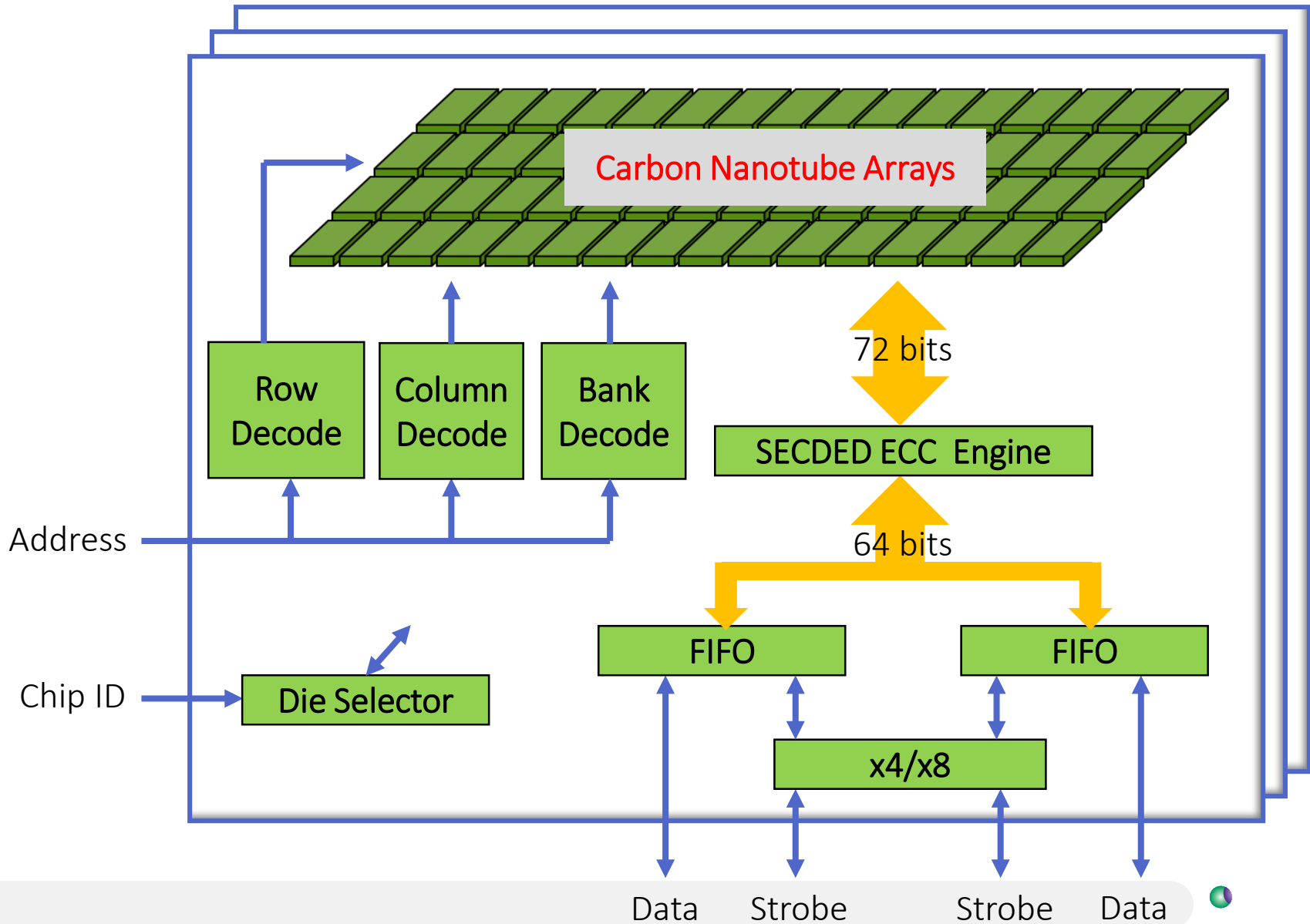
DDR4 NRAM

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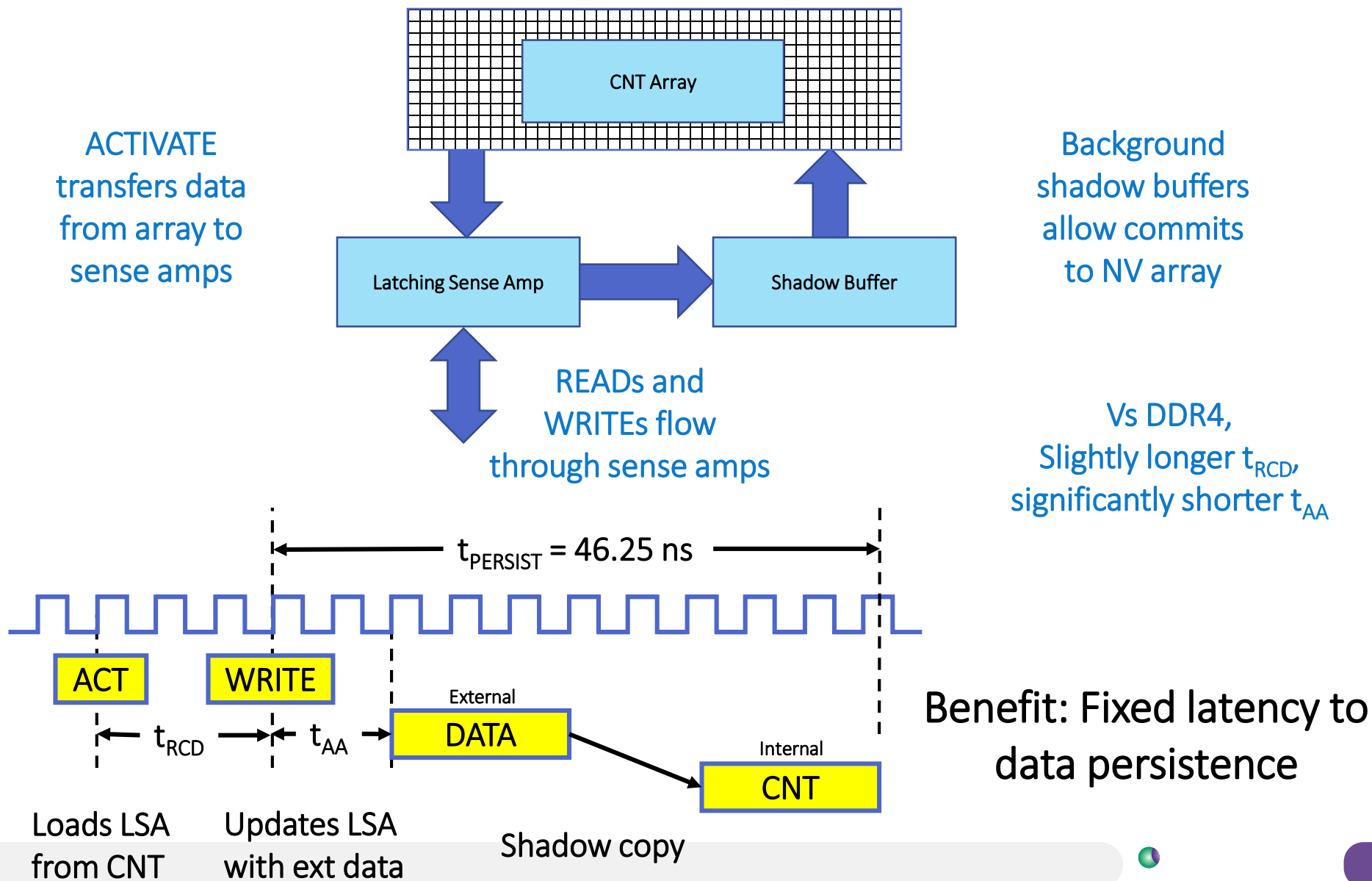




DDR4 NRAM Overview



Latching Sense Amps & Persistence Control



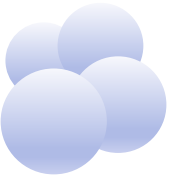
Timing Similar to DDR4E, Faster than DDR5

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Parameter		DDR4-2666-D 3DS	NRAM4-2666	DDR5-4400C
tRC	Activate to activate	47.00	46.25	50.18
tRCD	RAS to CAS	15.0	23.0	18.18
tAA	Read to data	17.14	13.5	18.18
tRP	Precharge	15.0	14.25	18.18
tRAS	Activate to precharge	32.0	32.0	32.0
tWR	Write recovery	15.0	23.0	45.0
tFAW	Four activate window limit	21.0	0	21.0
tRFC	Refresh time	550	0	295
_L / _S	Bank group to bank group	_S Slower	No penalty	_S Slower
3DS	Chip to chip in stack	2ck penalty	No penalty	4ck penalty

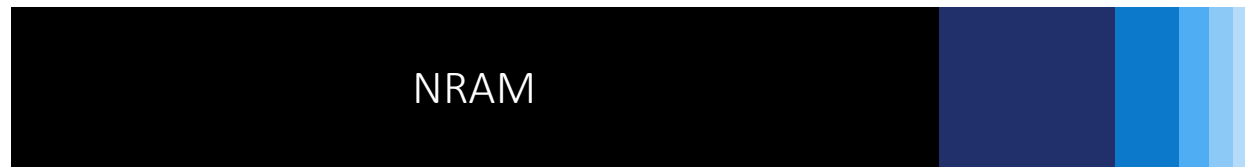
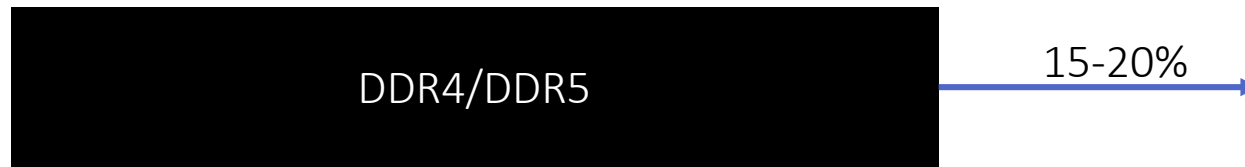
Latency: smaller is better





Bus Efficiency Comparison at Same Frequency

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Base throughput

Elimination of refresh

Elimination of tFAW restrictions

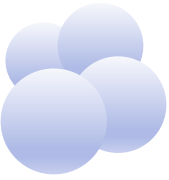
Elimination of bank group restrictions

Elimination of power states

Elimination of inter-die delays

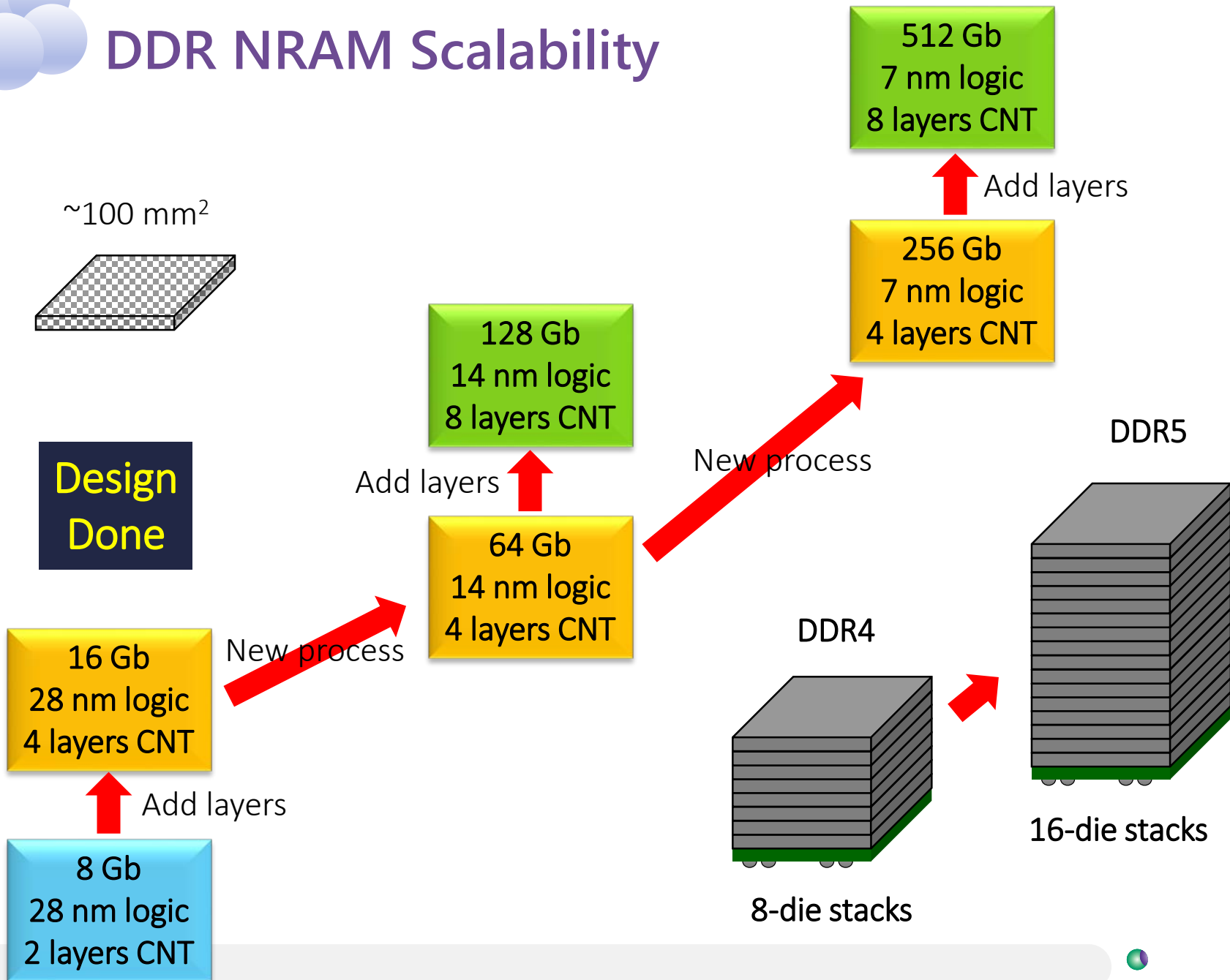
Architectural improvements
improve data throughput
15% or greater at the same
clock frequency

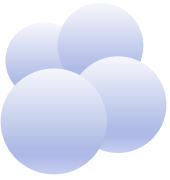




DDR NRAM Scalability

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Next Generation Main Memory Issues

A quick peek at DDR5 protocol reveals a dirty little secret...

Table 9 — 32 Gb Addressing Table

Configuration		8 Gb x4	4 Gb x8	2 Gb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
Row Address		R0~R16	R0~R16	R0~R16
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H	CID0~3 / 16H

Table 10 — 64 Gb Addressing Table

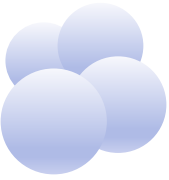
Configuration		16 Gb x4	8 Gb x8	4 Gb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
Row Address		R0~R17	R0~R17	R0~R17
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~2 / 8H	CID0~2 / 8H	CID0~2 / 8H

DDR5 bus is limited to $16H \times 32Gb = 8H \times 64Gb$

NRAM likely to scale to at least 256Gb/die in DDR5 timeframe

We need to correct this restriction in JEDEC





Driving Adoption of Higher Densities

JEDEC STANDARD

**DDR5 Non-Volatile Random Access
Memory (DDR5 NVRAM)**
Addendum #1 to JESD79-5

JESD79-5-1

JC-42 Item #1856.10

April 2019

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

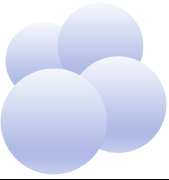


Nantero is chair of the JEDEC
Non-Volatile Memory Committee

Developing DDR5 NVRAM Specification



12 extended row bits enable up to 128Tb/die



Introducing “Memory Class Storage”

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